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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,198	10/28/2003	Chien-Ping Huang	60173 (71987)	7288
7590	10/13/2005		EXAMINER TRINH, HOA B	
Mr. Steven M. Jensen Mr. Peter F. Corless EDWARDS & ANGELL, LLP 101 Federal Street Boston, MA 02110			ART UNIT	PAPER NUMBER
			2814	
			DATE MAILED: 10/13/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/696,198

Applicant(s)

HUANG, CHIEN-PING

Examiner

Vikki H. Trinh

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claims Status*

1. Claims 1-8 are pending in this present application. Claims 9-18 have been canceled in the amendment filed on 08/02/05.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), figures 1-3, in view of Ho et al. (hereinafter Ho) (6,469,897).

APA discloses a multi-chip package device with a heat sink, comprising a chip carrier 20 (fig. 2); at least one first chip 11 (fig. 1) or 21 (fig. 2) mounted on and electrically connected to a surface of the chip carrier 20 (fig. 2); at least one semiconductor package 1,15 (fig. 1) or 22 (fig. 2) mounted on and electrically connected to the surface of the chip carrier 10 (fig. 1) or 20 (fig. 2); and the heat sink 24 (fig. 2) mounted via an adhesion layer 23 (fig. 2) on a surface of the first

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chip 21 (fig. 2) and a surface of the semiconductor package 22 (fig. 2) that are opposite to surfaces of the first chip 21 (fig. 2) and the semiconductor package 22 (fig. 2) mounted on the chip carrier 20 (fig. 2).

However, APA does not explicitly teach that at least one hollow part extending through the heat sink is formed at an area of the heat sink free of contact with the first chip and the semiconductor package to release thermal stresses from the heat sink.

Ho teaches a ball grid array package having a carrier 210(fig. 2D), a chip, and a heat sink 220 (fig. 2D) with a through-hole 222 (fig. 2B) formed in the area of the heat sink that is free from contacting a the chip (fig. 2D)

APA and Ho are in the same field of endeavors.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the heat sink of APA with a through-hole, as taught by Ho, so as to release heat from the package. Note that the through hole creates more surface area to the heat sink, thereby allowing heat to dissipate more or faster.

As to claim 2, APA teaches that the semiconductor package 2 (fig. 2) is a flip-chip ball grid array package (specification, page 3, line 11).

As to claim 3, APA teaches that the first chip 11 (fig. 1) is a graphic chip.

As to claim 4, APA teaches that the first chip 11 (fig. 1) is a graphic processing unit.

As to claim 6, APA teaches that the first chip 21 (fig. 2) is mounted at the center of the chip carrier 20 (fig. 2), and the semiconductor package 2 (fig. 2) is mounted at a position on the chip carrier 20 (fig. 2) corresponding to a corner of the heat sink 24 (fig. 2).

As to claim 7, the combined teaching of APA and Ho teaches that at least one pair of the semiconductor packages 22 (fig. 2) are mounted on the chip carrier 20 (fig. 2), and the hollow part 222 (fig. 2B, Ho) of the heat sink 220 (fig. 2D, Ho) is located between the semiconductor packages.

As to claim 8, at least one symmetrical pair 22 (fig. 2) of the hollow parts 222 (fig. 2B, Ho) are formed through the heat sink 220 (fig. 2B, Ho).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), figures 1-3, in view of Ho et al. (hereinafter Ho) (6,469,897), as applied to claim 1 above, and further in view of Behlen et al. (hereinafter Behlen) (5,598,033).

The combined teaching of APA and Ho discloses the invention substantially as claimed. However, APA and HO do not explicitly teach that the semiconductor package is a Random Access Memory (RAM) unit.

Behlen discloses a BGA package 300 (fig. 3) having a carrier 338, solder bumps 314 (fig. 3), and chip 310 (fig. 3), wherein the package is a volatile RAM (col. 1, line 13).

APA, Ho, and Behlen are in the same field of endeavors.

Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to modify the invention of APA and Ho with a RAM, as taught by Behlen, as merely a matter of selecting system for development.

***Response to Arguments***

6. Applicant's arguments filed 08/02/05 have been fully considered but they are not persuasive.

In response to applicant's argument that the Ho reference does not teach the feature as claimed, because Ho's through-hole is not hollow. On the contrary, as stated in the rejection, the through-hole 222(fig. 2B) of the heat sink 220 is hollow. Because of the hollow portion in the heat sink, the heat sink releases more heat due to the increase in the surface area. Similarly to the present invention, applicant claims a hollow portion through the heat sink to release more heat. Rather or not applicant decided later to fill the hollow portion in the heat sink is not yet being claimed. Therefore, Ho additional step of allowing the hollow portion be filled with solder material is not relevant to the present claims. So long Ho teaches a hollow portion in the heat sink at its intermediate product or final product, the product is still applicable to apply to the present claims. By the same token, applicant's claims may further include other subsequently steps before producing the final product. For the fore going reasons, the rejection is maintained.

**Conclusion**


7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.


8. Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for

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published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

9. Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site ([www.uspto.gov](http://www.uspto.gov)), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh,   
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**HOWARD WEISS**  
**PRIMARY EXAMINER**